Dolphin Technology

DOLPHIN TECHNOLOGY PRODUCT OFFERING
MEMORY COMPILERS

Dolphin provides a wide range of Memory Compilers and Specialty Memory (ROM, Multi Port RF, CAM, etc.) optimized to meet even the most demanding requirements for high performance, high density and low power.

The compilers enable SoC designers to generate macros with varying aspect ratios, redundancy schemes, VT variations and more.

SRAM & RF CATEGORY	2/3nm	4/5nm	6/7nm	12/16nm	22/28nm	40nm	55/65nm	80/90nm
High Performance - uses high current bit cells for high performance	●	●	●	●	●	●	●	●[1,2]
High Density - uses high-density bit cells to minimize area profile	●	●	●	●	●	●	●	●[1,2]
Ultra Low Leakage - significantly reduces leakage power while retaining all memory contents	●	●	●	●	●	●	●	●[1]
Dual Rail - reduces active and leakage power (periphery and array are run at separate voltages)	●	●	●	●	●	●	●	●
Power Gating - significantly reduces leakage power without retaining memory contents	●	●	●	●	●	●	●	●

SRAM & RF TYPE	2/3nm	4/5nm	6/7nm	12/16nm	22/28nm	40nm	55/65nm	80/90nm
Single Port SRAM - Up to 8K words deep, up to 288 bit wide, single instance up to 288 Kb					●	●	●	
Single Port SRAM - Up to 8K words deep, up to 320 bit wide, single instance up to 320 Kb	●	●	●					
Single Port SRAM - Up to 16K words deep, up to 288 bit wide, single instance up to 576 Kb						●[3]	●[3]	●
Single Port SRAM - Up to 16K words deep, up to 320 bit wide, single instance up to 640 Kb				●				
Pseudo Dual Port SRAM - Up to 8K words deep, up to 288 bit wide, single instance up to 288 Kb					●			
Pseudo Dual Port SRAM - Up to 8K words deep, up to 320 bit wide, single instance up to 320 Kb	●	●	●					
Pseudo Dual Port SRAM - Up to 16K words deep, up to 320 bit wide, single instance up to 640 Kb				●				
Dual Port SRAM - Up to 8K words deep, up to 288 bit wide, single instance up to 288 Kb					●	●	●	
Dual Port SRAM - Up to 8K words deep, up to 160 bit wide, single instance up to 160 Kb	●	●	●					
Dual Port SRAM - Up to 16K words deep, up to 144 bit wide, single instance up to 288 Kb						●[3]	●[3]	
Dual Port SRAM - Up to 16K words deep, up to 160 bit wide, single instance up to 320 Kb				●				
Dual Port SRAM - Up to 16K words deep, up to 288 bit wide, single instance up to 576 Kb								●
1 Port RF - Up to 1K words deep, up to 288 bit wide, single instance up to 72 Kb					●	●	●	●

Front End views are available under NDA.

For more information, contact Dolphin Support or sales@dolphin-ic.com

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1 Port RF - Up to 1K words deep, up to 640 bit wide, single instance up to 160 Kb	●	●	●					
1 Port RF - Up to 2K words deep, up to 640 bit wide, single instance up to 320 Kb				●				
2 Port RF - Up to 1K words deep, up to 288 bit wide, single instance up to 72 Kb					●	●	●	●
2 Port RF - Up to 1K words deep, up to 640 bit wide, single instance up to 160 Kb		●	●					
2 Port RF - Up to 2K words deep, up to 640 bit wide, single instance up to 320 Kb				●				

SPECIALTY MEMORY	2/3nm	4/5nm	6/7nm	12/16nm	22/28nm	40nm	55/65nm	80/90nm
Read Only Memory Compilers - Via Programmable and Diffusion	●	●	●	●	●	●	●	●
Content Addressable Memory Compilers - Binary BCAM, Ternary TCAM and CAM	●	●	●	●	●	●	●	●
Specialty Memory - Custom Register Files (4R/1W, 4R/2W, 3R/3W, 8R/1W, 5R/3W, etc.)	●R	●R	●R	●R	●R	●R	●R	●R

[1] SRAM Without Redundancy [2] RF 2-Port (1R/1W) [3] LP & ULP nodes only [R] Upon Request

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SRAM & RF FEATURES	2/3/4/5nm	7nm	12/16nm	22/28nm	40nm	55/65nm	80/90nm
Synchronous reads/writes	●	●	●	●	●	●	●
Static design with zero standby current (except transistor leakage)	●	●	●	●	●	●	●
Ability to compile to multiple aspect ratios	●	●	●	●	●	●	
RAMpiler+® with row and column redundancy of up to 2 quad rows & 2 columns I/O	●	●	●	●	●	●	●
No restriction and fully routable over the array with higher metal layers	●	●	●	●	●	●	●
Small set-up and zero hold times	●	●	●	●	●	●	●
Power ring size based on frequency of operation and load	●	●	●	●	●	●	●
Multiple pin placement and layer options	●	●	●	●	●	●	●
Multiple power ring metal layer and configuration options	●	●	●	●	●	●	●
Output enable	●	●	●	●	●	●	
Register output options							●
Register output options with scanning	●	●	●	●	●	●	
Pos. or Neg. Clock Edge	●	●	●	●	●	●	●
Multiple output drive strengths	●	●	●	●	●	●	●
Different power ring design configurations	●	●	●	●	●	●	●
Power ring based on frequency	●	●	●	●	●	●	●
Power Mesh on different Metal layers	●	●	●	●	●	●	●
Bit Write Mask, Byte Write or Word (global write) options	●	●	●	●	●	●	●
Write through, transparent write	●	●	●	●	●	●	●
Memory Test & Repair (BIST)	●	●	●	●	●	●	●
Memory Test & Repair (BIST) with XOR test inputs	●	●	●	●	●	●	
BIST Mux option on inputs	●	●	●	●	●	●	●
Row redundancy (RAMpiler+®)	●	●	●	●	●	●	●
Column I/O redundancy (RAMpiler+®)	●	●	●	●	●	●	●
Inputs isolation	●	●	●	●	●	●	
Low power option	●	●	●	●	●	●	
Ultra low leakage	●	●	●	●	●	●	
Fast option				●	●	●	
Power gating with and without data retention	●	●	●	●	●	●	
Dual rail option	●	●	●	●	●	●	
ECC enabled and capable (SEC, SECDED, OP, EP)	●	●	●	●	●	●	●

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MEMORY BIST

Dolphin Technology's Built-In Self-Test (BIST) solution supports all Dolphin memory compilers, including SRAM and RF.

MEMORY BIST	2/3/4/5nm	7nm	12/16nm	22/28nm	40nm	55/65nm	80/90nm
Fully automated MBIST RTL and Gate flow	●	●	●	●	●	●	●
Fully supported BIST test, diagnosis and soft/hard repair	●	●	●	●	●	●	●
Fully supported eFuse controller for automated hard repair	●	●	●	●	●	●	●
Analyze RTL design or netlist to identify memories	●	●	●	●	●	●	●
Plan MBIST engines	●	●	●	●	●	●	●
Verify stand-alone	●	●	●	●	●	●	●
Insert into RTL design or netlist	●	●	●	●	●	●	●
Verify partition level	●	●	●	●	●	●	●
Top level hookup to JTAG	●	●	●	●	●	●	●
Fully supported P1500 interface and Tap controller	●	●	●	●	●	●	●
Verify top level	●	●	●	●	●	●	●

MEMORY BIST	2/3/4/5nm	7nm	12/16nm	22/28nm	40nm	55/65nm	80/90nm
Generate test patterns and SVF file	●	●	●	●	●	●	●
Incremental repair capability	●	●	●	●	●	●	●
Programmable March-style algorithm	●	●	●	●	●	●	●
APB interface for BIST test and fuse operation	●	●	●	●	●	●	●
Diagnosis test, Characterization test and SVF debug flow	●	●	●	●	●	●	●
Fully supported ICL/PDL of IEEE 1687	●	●	●	●	●	●	●
Automated subchip integration flow	●	●	●	●	●	●	●

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